ABSTRACT OF THE DISCLOSURE

A method and apparatus for clearing the memory of an FPGA IC, when the IC is comprised of a plurality of cores. The system comprises the acts of clearing the memory of the plurality of cores; sequentially verifying completion of act of clearing memory act for each core; and providing a programming ready signal to all cores when a last core has completed said clearing memory act. A method and apparatus for sequentially programming with bitstream data each core of a plurality of cores in an FPGA IC, said method comprising: sending the bitstream data to a first core of the plurality of cores; sending the balance of the bitstream data to a next core of the plurality of cores after the first core has received its portion of bitstream data; repeating in a sequential manner the acts of sending a balance of the bitstream data to a following core of the plurality of cores after an immediately preceding core of has received its portion of bitstream data, until a last core of the plurality of cores has received its portion of bitstream data; and sending a program start signal to all cores, after a last core has received its portion of the bitstream data. It is emphasized that this abstract is provided to comply with the rules requiring an abstract that will allow a searcher or other reader to quickly ascertain the subject matter of the technical disclosure. It is submitted with the understand that it will not be used to interpret or limit the scope or meaning of the claims. 37 CFR 1.72(b).

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